

Remarks

1. Applicant appreciates the Examiner's thorough review of the present application, and respectfully requests reconsideration in light of the foregoing amendments and the following remarks.

2. Claims 12-20 are pending in the application as claims 1-11 were cancelled by applicant's amendment and response to restriction requirement.

3. Reconsideration and allowance of amended independent claim 12 are respectfully requested in light of the foregoing amendments and the following remarks. Claims 13-20 ultimately depend on amended claim 12, and therefore are considered to be in condition for allowance.

4. The amendments to claims 17, 18, 19, and 20 define the claimed invention more clearly and clarify the distinctions between the claimed invention and the cited references.

The claimed invention (one embodiment of which is illustrated in Fig. 6) differs from U.S. Patent No. 6,281,581 in at least the ways described below.

The second part 610 according to the prior art connects the first part 612 and 614 in series to form an interconnection portion between the device carrier 604 and the semiconductor unit 606, i.e., the second part 610, and the first part 612 and 614 are connected in series to form the interconnection portion. In contrast, both the first part 3 and the second part 5 of an interconnection portion according to the claimed invention respectively span between the device carrier 7 and the semiconductor unit 2, i.e., the first part 3 and the second part 5 are connected in parallel to form an interconnection portion between the device carrier 7 and the semiconductor unit 2.

Another difference between the claimed invention and the prior art is the area of surface of the second part for connecting the first part. The second part 610 according to the prior art has only part of its surface connected to the first part 612 and 614, and thereby is mostly exposed. In contrast, the second part 5 of an interconnection portion according to the claimed invention is wrapped by the first part 3 of the interconnection portion, and thereby is not exposed.

A further difference between the claimed invention and the prior art is in the objects of these inventions. The object of the prior art is to provide a solution to a problem (lines 11-26 of col 2, Fig. 3): a crack 34 resulting from thermal fatigue is formed between a solder joint and a corresponding pad 33 of a device carrier 32. In contrast, one objective of the embodiment of the present invention recited in claim 12 is to provide a solution to a problem (lines 14-21 of page 1): in conventional methods connecting a chip via bumps to a lead frame or a device carrier having neither connection pads nor insulation layer thereon, a reflow soldering (heat applying) process always results in bumps' collapses of inconsistent height due to disunity of wetting (or solder flowing) on the surface of such a device carrier because no mechanism is provided to limit the solder flow. Another object of the embodiment claimed in claim 12 is to solve another problem: in conventional methods of connecting a chip via bumps to a lead frame or a device carrier having neither connection pads nor insulation layer thereon, the chip contacts the device carrier as a result of bumps' collapses of inconsistent height due to disunity of wetting (or solder flowing) on the surface of such a device carrier.

The claimed invention (one embodiment of which is illustrated in Fig. 6) differs from U.S. Patent No. 6,506,671 in the ways described below.

The second part (solder ball 20') of an interconnection portion between a semiconductor device 10 and a substrate 30 according to the prior art is partially surrounded by the first part

(ring 50'), wherein the first part (ring 50') includes aperture 52 and has a melting point higher than that of the second part (solder ball 20'). In contrast, the second part 5 of an interconnection portion between a semiconductor unit 2 and a device carrier 7 according to the claimed invention is wrapped by the first part 3, wherein the first part 3 has a melting point lower than that of the second part.

The melting point of the first part (ring 50') according to the prior art is higher than that of the second part (solder ball 20') is established by the following statements cited therefrom: "Since the ring protrudes from the surface of the semiconductor device component, when a solder ball is bonded or otherwise secured to the contact pad exposed through the ring, the ring laterally surrounds at least a portion of the solder ball...." in lines 63-67 of col 3 and lines 1-5 of col 4; "Another significant advantage of the rings of the present invention is the containment of the solder of the balls, in the manner of a dam, during solder reflow, thus preventing contamination of the passivation layer surrounding the contact pads" in lines 17-21 of col 4; "Each ring 50 defines an aperture 52 through which at least a portion of the surrounded contact pad 12 is exposed. Each ring 50 protrudes from surface 14 of semiconductor device 10 so as to laterally surround and contact at least a portion of a solder ball to be bonded or otherwise secured to bond pad 12 and to support that portion of the solder ball to prevent fatigue thereof during thermal cycling of semiconductor device 10" in lines 45-52 of col 5; "As shown in FIG. 5, solder ball 20' extends through an aperture 52' of ring 50' to contact pad 12" in lines 26-27 of col 6; and "rings 50' prevent material of solder balls 20' from contacting surface 14 of semiconductor device 10" in lines 37-38 of col 6. The melting point of the first part (ring 50') according to the prior art must be higher than that of the second part (solder ball 20') if the statements above are true.

Another difference between the claimed invention and the prior art is the distance between the first part of an interconnection portion and the device carrier. There is a distance between the first part (ring 50') and the device carrier (substrate 30) according to the prior art because the first part (ring 50') is fabricated before the semiconductor device 10 is connected to the substrate 30 via the second part (solder ball 20'). In contrast, both the first part 3 and the second part 5 according to the claimed invention span between the device carrier 7 and the semiconductor unit 2, and there is no distance between the first part 3 and the device carrier 7. This results from the fact that the first part 3 is formed in the process of connecting the semiconductor unit 2 with the device carrier 7.

A further difference between the claimed invention and the prior art is that the object of the prior art is to provide a solution to a problem (lines 44-60 of col 1): expansion and contraction resulting from thermal cycling during manufacturing and testing process are serious at the interface between a solder ball and a contact pad of a semiconductor device, causing solder fatigue, reducing the strength of the solder balls, resulting in cracking and failure of the solder balls, and diminishing the reliability of the solder balls as mechanical and electrical connection elements. In contrast, one object of the embodiment recited in claim 12 is to provide a solution to a problem (lines 14-21 of page 1): in conventional methods of connecting a chip via bumps to a lead frame or a device carrier having neither connection pads nor insulation layer thereon, the reflow soldering (heat applying) process always results in bumps' collapses of inconsistent height due to disunity of wetting (or solder flowing) on the surface of such a device carrier, because no mechanism is provided to limit the solder flow. Another object of the embodiment of the invention recited in claim 12 is to provide a solution to another problem: in conventional methods of connecting a chip via bumps to a lead frame or a device carrier having neither

connection pads nor insulation layer thereon, the chip contacts the device carrier as a result of bumps' collapses of inconsistent height due to disunity of wetting (or solder flowing) on the surface of such a device carrier.

A feature, i.e., that the first part 3 spans between the metal surface 72 and the semiconductor unit 2, and the second part 5 spans between the metal surface 72 and the electrode 26 of said semiconductor unit 2, is now added to claim 12. The added feature, together with the future "said first part having a melting point lower than that of said second part and adhering to said second part" in the original claim 12, are not anticipated or suggested by the combination of U.S. Patent 6,281,581, U.S. Patent 6,506,671, and the other prior art of which applicant is aware.

Moreover, another feature, i.e., that the second part 5 is wrapped by the first part 3, is now added to claim 12. This added feature further distinguishes claim 12 from the combination of U.S. Patent 6,281,581, U.S. Patent 6,506,671, and the prior art of which applicant currently is aware.

The features that "said first part spanning between said metal surface and said semiconductor unit, said second part spanning between said metal surface and the electrode of said semiconductor unit, said second part being wrapped by said first part" as added to claim 12 are supported by Figs. 6, 7b, and 12, lines 4-7 and lines 26-28 of page 7, lines 25-28 of page 17, and lines 1-6 of page 18 of the present application.

The features included in amended independent claim 12 are neither anticipated nor suggested by the combination of U.S. Patent 6,281,581, U.S. Patent 6,506,671, and the prior art of which applicant currently is aware.

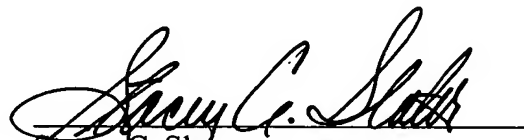
Accordingly, amended claim 12 overcomes the Examiner's rejections under 35 U.S.C. 103(a), is in condition for allowance and such action is respectfully requested. Original claims

13-16, and amended claims 17-20, ultimately depend on amended claim 12. These claims are allowable for the reasons stated herein, and further in view of the patentable combination of features recited in such dependant claims. The present application therefore is in condition for allowance and such action is respectfully requested.

Respectfully submitted,

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